

# M3302A PXIe Arbitrary Waveform Generator and Digitizer with Optional Real-Time Sequencing and FPGA Programming

500 MSa/s, 16 Bits, 2 Channel Arbitrary Waveform Generator

500 MSa/s, 14 Bits, 2 Channel Digitizer



## Applications

General purpose AWGs and digitizers

High-performance control

Communications: BB/IF SDR, channel emulation, transceiver testing

Aerospace and defense (A/D): RADAR, electronic warfare (EW)

Hardware-in-the-loop (HIL), automated test equipment (ATE)

Scientific research

Quantum computing



### Fast, Flexible, High-Performance Control, Testing & Prototyping

The M3302A modules provide the ideal tool for testing and prototyping in control or communications applications. Performance meets simplicity, thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI), and graphical FPGA programming technology.

## Features

### Outputs (AWG)

- 500 MSa/s, 16 Bits, 2 Channels

### Output features

- AWGs, function generators, AM/FM/PM modulators
- Advanced triggering and marking functionalities

### Inputs (Digitizer)

- 500 MSa/s, 14 Bits, 2 Channels

### Input features

- Powerful data acquisition system (DAQ)
- Advanced triggering and marking functionalities

### Less than 400 ns input to output latency

### Optional HW programming for high-performance applications

- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7K410T FPGA

### Up to 2 GB of onboard RAM (~ 1 Gsamples)

### Mechanical/interface

- 2 slots 3U (PXIe)
- PCIe Gen1
- Independent DMA channels for fast and efficient data transfer

# Functional Block Diagrams

## Output — Arbitrary Waveform Generator

Note that all channels have identical output structure.

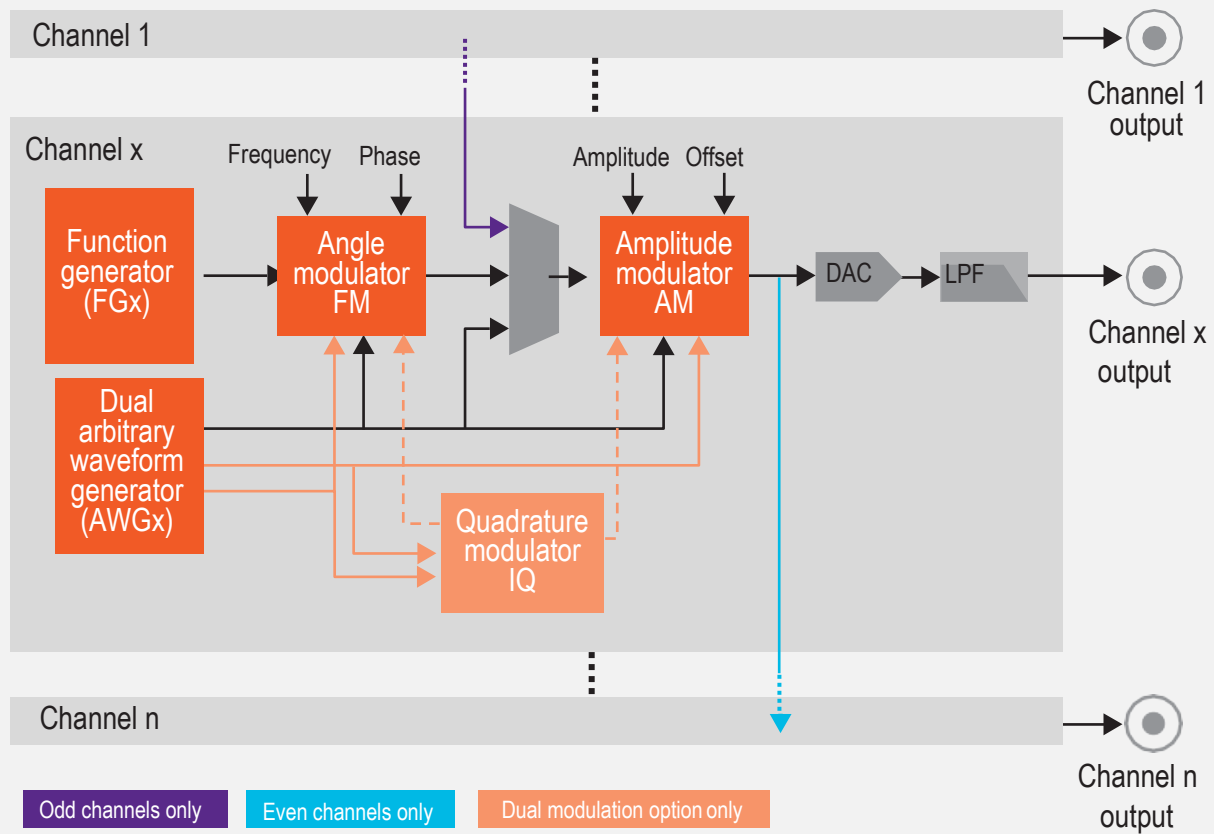


Figure 1. M3302A output functional block diagram. Source: [Keysight.com](https://www.keysight.com)

## Input — Digitizer

Note that all channels have identical input structure.

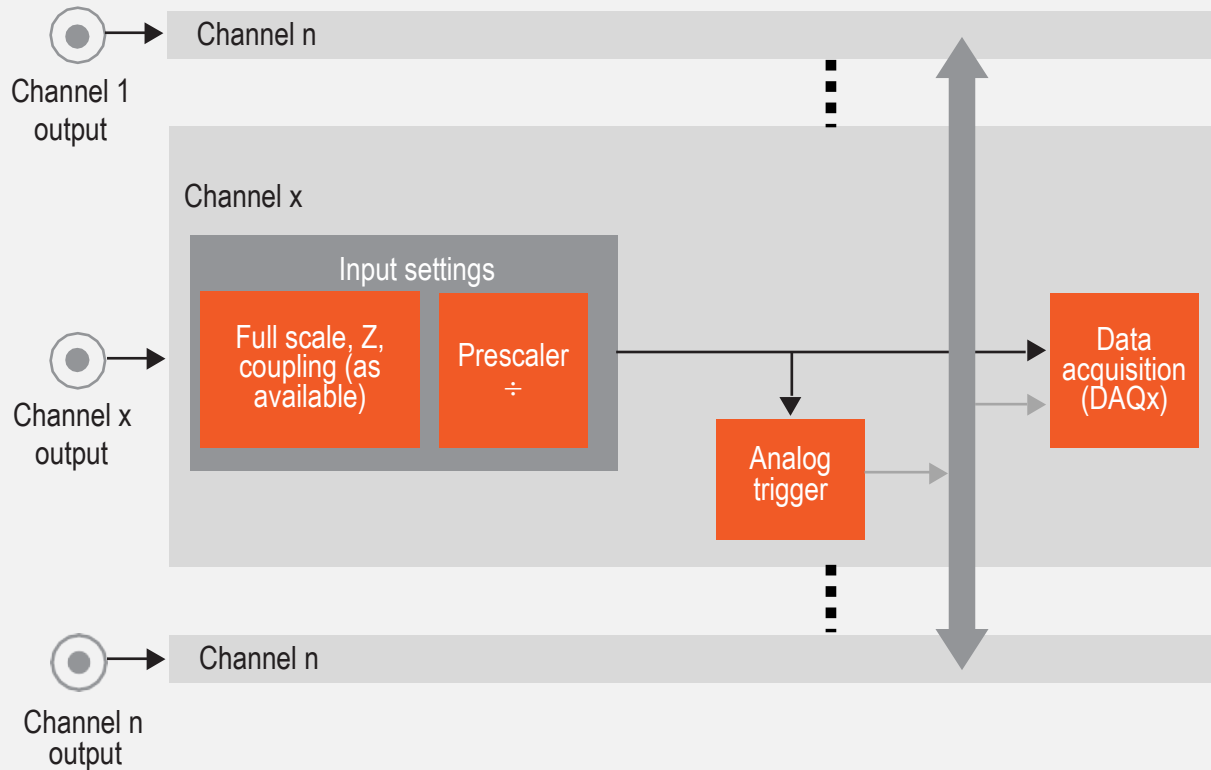


Figure 2. M3302A input functional block diagram. Source: [Keysight.com](https://www.keysight.com)

## Programming Technology and Software Tools

### Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python

### Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully parallel, hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization and data exchange
- FPGA programming
  - FPGA design environment and BSP support
  - Supports VHDL, Verilog and Xilinx projects, and Xilinx IP Catalog
  - Ultra-fast, one-click compiling and on-the-fly programming

## SD1 2.x and SD1 3.x differences

Keysight SD1 2.x software has been upgraded to 3.x. The key differences are listed in the table below. For more detail on SD1 3.x software, refer to the [Start Up Guide M3xxx-90002](#).

**WARNING**

**The 3.X version of software does not support programs using the M3601A or the M3602A applications. You will have to transition to KS2201A and KF9000A respectively.**

SD1 Features	Legacy (SD1 2.1.x)	New (SD1 3.x)
<b>Software</b>		
Design Environment	M3601A HVI design environment (ProcessFlow)	KS2201A PathWave Test Sync Executive (HVI2 technology)
	M3602A FPGA design environment (FPGAFlow)	KF9000A PathWave FPGA Programming Environment (commonly known as PathWave FPGA)
HVI Technology <sup>1</sup>	<ul style="list-style-type: none"> <li>Graphical M3601A for HV1</li> <li>HVI-C API (through SD1 installer)</li> </ul>	KS2201A PathWave Test Sync Executive (HVI2 Core API through a separate HVI installer)
FPGA Programming	<ul style="list-style-type: none"> <li>Graphical M3602A FPGA Designing (BSP for SD1 2.1.x only)</li> </ul>	KF9000A PathWave FPGA (BSP installer for each supported module is required)
Soft Front Panel (SFP)	Available	Available
Programming Interface	Python <sup>1</sup> , C++, C#, LabVIEW, MATLAB	Python <sup>1</sup> , C, C++, C#, LabVIEW, MATLAB
Supported Operating System	Windows 10 (32 / 64 bit)	Windows 10 (x64 bit)
<b>Hardware modules</b>		
M3202A (AWG 1G)	FW version<4.0 (CH2* or CH4) (CLF / CLV) (K16, K32, K41) BSP available (K32,K41)	FW version>=4.0 (CH4) (CLF / CLV**) (K16, K32, K41) BSP available(K32, K41)
M3201A (AWG 500)	FW version<4.0 (CH2* or CH4) (CLF / CLV) (K16, K32, K41) BSP available (K32, K41)	FW version>=4.0 (CH4) (CLF / CLV**) (K16, K32, K41) BSP available (K32, K41)

SD1 Features	Legacy (SD1 2.1.x)	New (SD1 3.x)
M3102A (DIG 500)	FW version<2.0 (CH2* or CH4) (CLF / CLV*) (K16, K32, K41) BSP available (K32, K41)	FW version>=2.0 (CH4) (CLF) (K16, K32, K41) BSP available(K32, K41)
M3100A (DIG 100)	FW version<2.0 (CLF / CLV*) (CH4 or CH8) (K16, K32, K41) BSP available (K32, K41)	FW version>=2.0 (CLF) (CH4 or CH8) (K32, K41) BSP available (K32, K41)
M3302A (COMBO 500 500)	FW version<4.0 (CLF / CLV*) (CH2 AWG–CH2 DIG) (K32*, K41) BSP available (K32*, K41)	FW version>=4.0 (CLF) (CH2 AWG–CH2 DIG) (K41) BSP available (K41)
M3300A (COMBO 500 100)	FW version<4.0 (CLF) (CH2 AWG–CH4 DIG or CH4 AWG–CH8 DIG) (K16*, K32*, K41) BSP available (K32*)	FW version>=4.0 (CLF) (CH2 AWG–CH4 DIG or CH4 AWG–CH8 DIG) (K41) BSP available (K41)
<b>No programming</b>		
Easily configurable SD1 SFP (software front panel) interface for each connected module.		

<sup>1</sup> HVI programming with supported with Python version 3.7 only.

\* This Hardware Option cannot be procured. Contact [Keysight Support](#) for more information.

\*\* Only Default Clock Speed is supported. Variable Clock is NOT supported.

## PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Output (AWGs)				Input (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	4	DC-400				
M3201A	AWG	500	16	4	DC-200				
M3102A	Digitizer					500	14	4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	DC-200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	DC-200	100	14	4/8	DC-100

# AWG Technical Specifications and Characteristics

## General characteristics

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>Inputs and Outputs</b>					
Channels (single-ended mode)		2		Out	
Channels (differential mode)		1		Out	Differential uses 2 channels
Reference clock <sup>1</sup>		1		Out	
Reference clock <sup>2</sup>		1		In	
Triggers/markers <sup>1,3</sup>		1		In/Out	Reconfigurable
Triggers/markers <sup>2,3</sup>		8		In/Out	Reconfigurable
<b>Output channels overview</b>					
Sampling rate <sup>4</sup>	0.005		500	Msa/s	
Voltage resolution		16		Bits	
Output frequency	DC		200	MHz	
Real-time BW			200	MHz	
Output voltage	-1.5		1.5	Volts	
<b>Built-in functionalities</b>					
Function generators		2			1 per channel
Dual AWGs		2			1 per channel
IQ modulators		2			1 per channel
Frequency modulators		2			1 per channel
Phase modulators		2			1 per channel
Amplitude modulators		2			1 per channel
DC offset modulators		2			1 per channel
<b>Onboard memory</b>					
RAM memory	16		2048	MBytes	

1. At front panel.

2. At backplane.

3. Markers available from SD1 software version 3.0 onwards.

4. (-CLF) option: fixed 500 MSa/s.

## I/O Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>Output channels</b>					
Sampling rate <sup>1</sup>	100		500	MSa/s	
Output frequency	0		200	MHz	Limited by a reconstruction filter
Output voltage	-1.5		1.5	Volts	On a 50 Ω load
Source impedance		50		Ω	
<b>Reference clock output</b>					
Frequency		10 to 12.5 <sup>2</sup>		MHz	Generated from the internal clock, user selectable
Voltage		800		mV <sub>pp</sub>	On a 50 Ω load
Power		2		dBm	On a 50 Ω load
Source impedance		50		Ω	AC coupled
<b>External I/O trigger/marker</b>					
V <sub>IH</sub>	2		5	V	
V <sub>IL</sub>	0		0.8	V	
V <sub>OH</sub>	2.4		3.3	V	On a high Z load
V <sub>OL</sub>	0		0.25	V	On a high Z load
Input impedance		10		KΩ	
Source impedance		TTL		-	
Speed		100		MHz	

1. (-CLF) option: fixed 500 MSa/s.

2. CLF option is set to 10 MHz.



## Function Generators (FGs) Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General specifications</b>					
Function generators		2			1 per channel
Waveform types		4			Sinusoidal, triangular, square and DC
Frequency range	0		200	MHz	
Frequency resolution		45		Bits	
Frequency resolution		5.7		μHz	
Phase range	0		360	Deg	
Phase resolution		24		Bits	
Phase resolution		21.5		μdeg	
<b>Reference clock output</b>					
Frequency change rate		100		MChanges/s	With HVI technology
Frequency modulation rate		500		MSamples/s	With AWGs and angle modulators
Phase change rate		100		MChanges/s	With HVI technology
Phase modulation rate		500		MSamples/s	With AWGs and angle modulators

## Amplitude and Offset Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General specifications</b>					
Amplitude/offset range	-1.5		1.5	Volts	Amplitude + offset values
Amplitude/offset resolution		16		Bits	
Amplitude/offset resolution		45.8		μV	
<b>Reference clock output</b>					
Amplitude/offset change rate		500		MChanges/s	With HVI technology
Amplitude/offset modulation rate		500		MSamples/s	With AWGs and angle modulators

## Arbitrary Waveform Generators (AWGs) Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General specifications</b>					
Dual AWGs		2			1 Dual AWG per output channel
Aggregated speed (16 bits)			2000	MSa/s	For all onboard waveforms combined
Aggregated speed (32 bits)			1000	MSa/s	For all onboard waveforms combined
Waveform multiple		5		Samples	Waveform length must be a multiple of this value
16-bit waveform length	65		957M	Samples	Maximum depends on onboard RAM
32-bit waveform length	65		478M	Samples	Maximum depends on onboard RAM
Waveform length efficiency		93.5		%	Efficiency = waveform size/waveform size in RAM
Trigger		Select			External Trigger (input connector, backplane triggers), SW/HVI trigger
<b>AWG specifications (16-bit single waveform)</b>					
Speed			500	MSa/s	Per AWG
Resolution		16		Bits	
AWG destination		Select			Amplitude, offset, frequency or phase
<b>AWG specifications (16-bit dual waveform)</b>					
Speed (waveform A)			500	MSa/s	Per AWG
Speed (waveform B)			500	MSa/s	Per AWG
Resolution (waveform A)		16		Bits	
Resolution (waveform B)		16		Bits	
AWG destination (waveform A)		Select			Amplitude and offset or I and Q control outputs on channels 1,2
AWG destination (waveform B)		Select			Frequency and phase or I and Q readouts on channels 3,4

## Angle Modulators Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General specifications</b>					
Frequency modulators		2			1 per output channel
Phase modulators		2			1 per output channel
Carrier signal source		FGs			refer FG specifications table in this document
Modulating signal source		AWGs			refer AWG specifications table in this document
<b>Frequency modulators (16-bit modulating waveform)</b>					
Deviation	-Dev. Gain		+Dev. Gain	MHz	
Modulating signal resolution		16		Bits	AWG waveform
Modulating signal BW	0		250	MHz	AWG Nyquist limit
Deviation gain	0		200	MHz	
Deviation gain resolution		16		Bits	
<b>Phase modulators (16-bit modulating waveform)</b>					
Deviation	-Dev. Gain		+Dev. Gain	Deg	
Modulating signal resolution		16		Bits	AWG waveform
Modulating signal BW	0		250	MHz	AWG Nyquist limit
Deviation gain	0		180	Deg	
Deviation gain resolution		16		Bits	~ 5.5 mdeg

## Amplitude Modulators Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General specifications</b>					
Amplitude modulators		2			1 per output channel
Offset modulators		2			1 per output channel
Carrier signal source		FGs			refer FG specifications table in this document
Modulating signal source		AWGs			refer AWG specifications table in this document
<b>Amplitude and offset modulators (16-bit modulating waveform)</b>					
Deviation	-Dev. Gain		+Dev. Gain	V <sub>p</sub>	
Modulating signal resolution		16		Bits	AWG waveform
Modulating signal BW	0		250	MHz	AWG Nyquist limit
Deviation gain	0		1.5	V <sub>n</sub>	
Deviation gain resolution		16		Bits	Limited by the output DAC

## IQ Modulators Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General specifications</b>					
IQ modulators		2			1 per output channel
Carrier signal source		FGs			refer FG specifications table in this document
Modulating signal source		AWGs			refer AWG specifications table in this document
<b>External I/O trigger/marker</b>					
Amplitude deviation	-1.5		+1.5	V <sub>p</sub>	
Phase deviation	-180		180	Deg	
I modulating signal resolution		16		Bits	AWG waveform
I modulating signal BW	0		250	MHz	AWG Nyquist limit
Q modulating signal resolution		16		Bits	AWG waveform
Q modulating signal BW	0		250	MHz	AWG Nyquist limit

## Clock System Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General specifications</b>					
Clock Frequency (-CLF)		500		MHz	Fixed Clock

## AC performance

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>General characteristics</b>					
Analog output jitter		< 2		ps	RMS (cycle-to-cycle)
AWG trigger to output jitter		< 2		ps	RMS (cycle-to-cycle) for any trigger referenced to the chassis clock; independent of input trigger jitter if input jitter < 4ns peak-to-peak
Trigger resolution		10		ns	
Channel-to-channel skew		< 20		ps	Between ch 0 and ch 1, and ch 2 and ch 3
		< 50		ps	Between any channel
		< 150		ps	Between modules, chassis dependent <sup>2</sup>
Clock output jitter		< 2		ps	RMS (cycle-to-cycle)
Clock accuracy and stability		100		ppm	PXle, PCIe versions; chassis dependent <sup>1</sup>
<b>AC characteristics</b>					
Spurious-free dynamic range (SFDR)					
					$P_{out} = 4 \text{ dBm}$ , measured from DC to max frequency
$f_{out} = 10 \text{ MHz}$		68		dBc	
$f_{out} = 80 \text{ MHz}$		64		dBc	
$f_{out} = 120 \text{ MHz}$		57		dBc	
$f_{out} = 160 \text{ MHz}$		54		dBc	
Crosstalk (adjacent channels)					
$f_{out} = 10 \text{ MHz}$		< -105		dB	
$f_{out} = 80 \text{ MHz}$		-75		dB	
$f_{out} = 120 \text{ MHz}$		-88		dB	
$f_{out} = 160 \text{ MHz}$		-73		dB	

## M3302A-C22

## Crosstalk (non-adjacent channels)

$f_{out} = 10 \text{ MHz}$		< -105		dB	
$f_{out} = 80 \text{ MHz}$		-78		dB	
$f_{out} = 120 \text{ MHz}$		< -105		dB	
$f_{out} = 160 \text{ MHz}$		-92		dB	

## Phase noise (SSB)

offset = 1 KHz		< -127		dBc/Hz	
offset = 10 KHz		< -133		dBc/Hz	
offset = 100 KHz		< -138		dBc/Hz	

## Average noise power density

		< -145		dBm/Hz	
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1. This value corresponds to a M9505A chassis. This value can be improved with an external chassis clock or a system timing module.
2. This value corresponds to a M9005A PXIe chassis.

## AC performance, typical

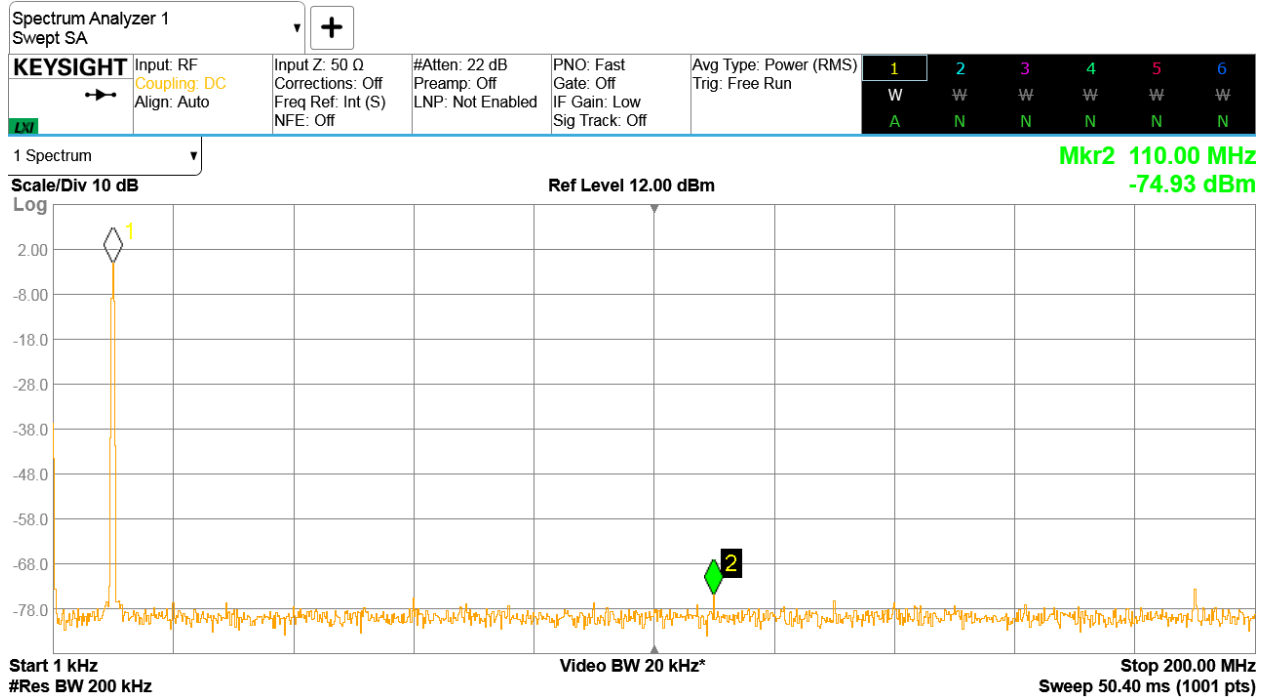


Figure 3. Single-tone spectrum at  $f_{out} = 10$  MHz. Source: [Keysight.com](http://Keysight.com)

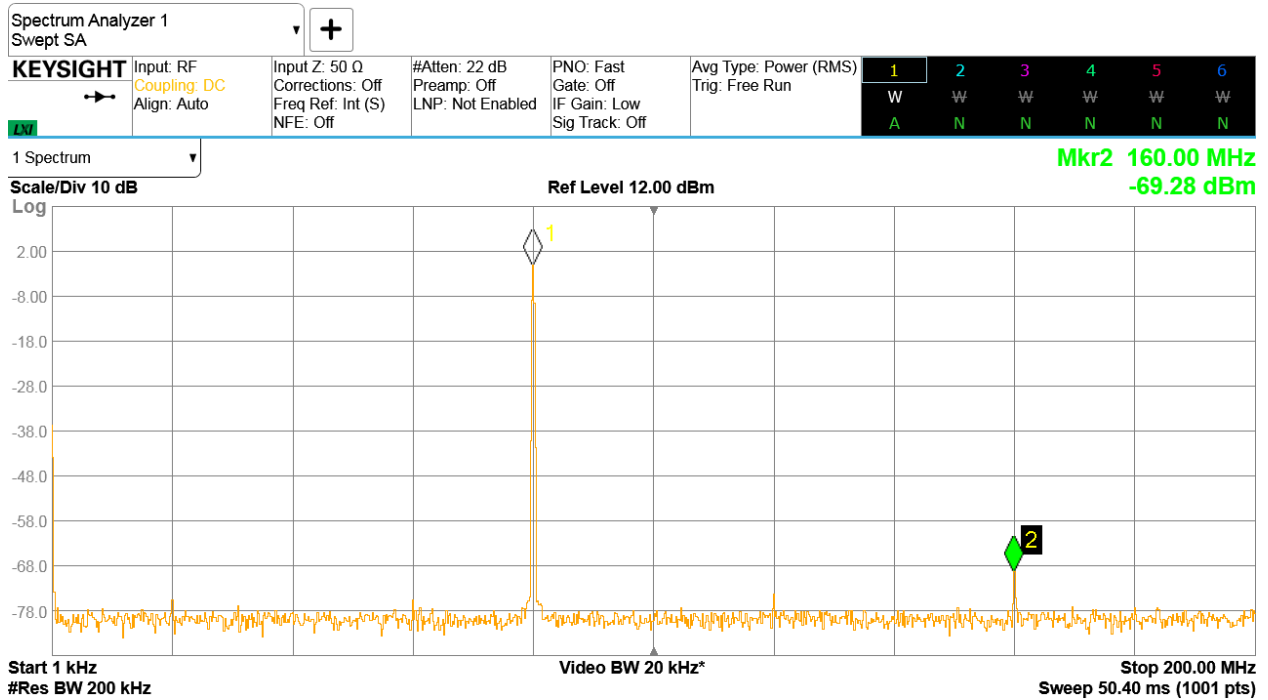


Figure 4. Single-tone spectrum at  $f_{out} = 80$  MHz. Source: [Keysight.com](http://Keysight.com)

## AC performance, typical

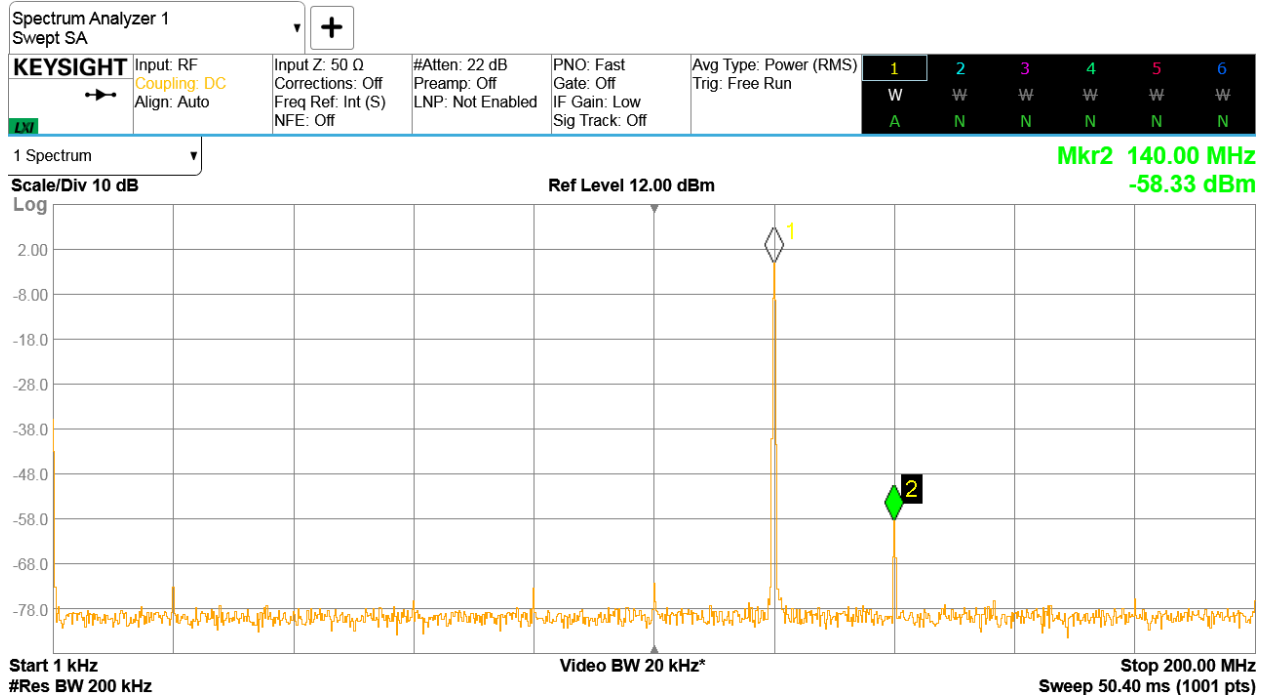


Figure 5. Single-tone spectrum at  $f_{out} = 120$  MHz. Source: [Keysight.com](http://Keysight.com)

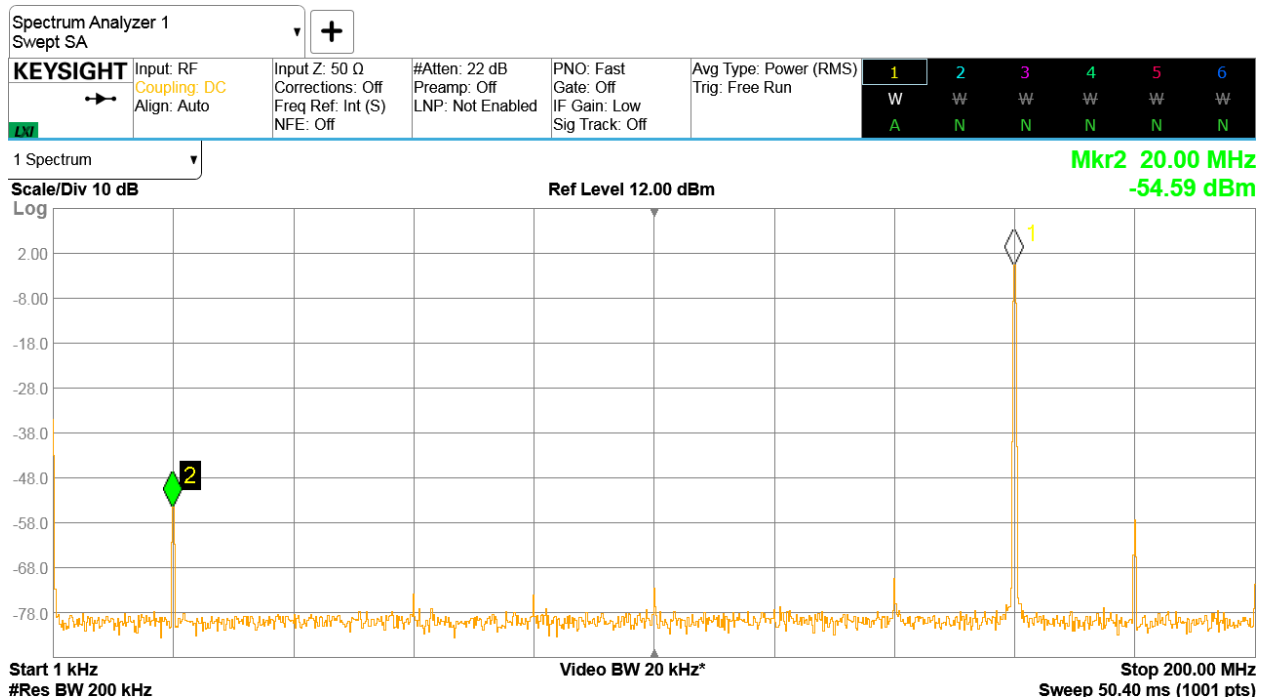


Figure 6. Single-tone spectrum at  $f_{out} = 160$  MHz. Source: [Keysight.com](http://Keysight.com)



# Digitizer Technical Specifications and Characteristics

## General characteristics

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>Inputs and Outputs</b>					
Channels		2		Out	
Reference clock <sup>1</sup>		1		Out	
Reference clock <sup>2</sup>		1		In	
Triggers/markers <sup>1,3</sup>		1		In/Out	Reconfigurable
Triggers/markers <sup>2,3</sup>		8		In/Out	Reconfigurable
<b>Output channels overview</b>					
Sampling rate <sup>4</sup>		500		Msa/s	
Voltage resolution		14		Bits	
Output frequency	0		200	MHz	
Real-time BW		200		MHz	
Time Skew		< 50		ps	Between channels
<b>Built-in functionalities</b>					
Input conditioning blocks		2			1 per channel
Analog trigger processors		2			1 per channel
Data acquisition blocks		2			1 per channel
<b>Onboard memory</b>					
RAM memory	16		2048	MBytes	

1. At front panel.
2. At backplane.
3. Markers available from SD1 software version 3.0 onwards.
4. (-CLF) option: fixed 500 MSa/s.

## I/O Specifications

Analog input characteristics	
Number of channels	C22
Sampling rate	500 MSa/s option -CLF
Configurable inputs: impedance	50 $\Omega$ or 1 M $\Omega$ (HiZ)
Configurable inputs: Coupling	AC or DC
Input voltage range (50 $\Omega$ )	125 mV <sub>pp</sub> to 8 V <sub>pp</sub> (7 scales: 0.125, 0.25, 0.5, 1, 2, 4, 8 V <sub>pp</sub> )
Input voltage range (HiZ)	200 mV <sub>pp</sub> to 16 V <sub>pp</sub> (7 scales: 0.2, 0.4, 0.8, 2, 4, 8, 16 V <sub>pp</sub> )
Bandwidth limit filters	200 MHz
Effective number of bits (ENOB) <sup>1</sup>	10.6 bits at 95 MHz (typical)
Noise floor <sup>1</sup>	-146 dBm/Hz
SINAD <sup>1</sup>	66 dB at 95 MHz (typical)
Spurious free dynamic range (SFDR) + Total Harmonic Distortion <sup>1</sup>	71 dBc at 95 MHz (typical)

<sup>1</sup> Measured at -1 DBFS input signal with 1 V<sub>pp</sub> 50  $\Omega$ .

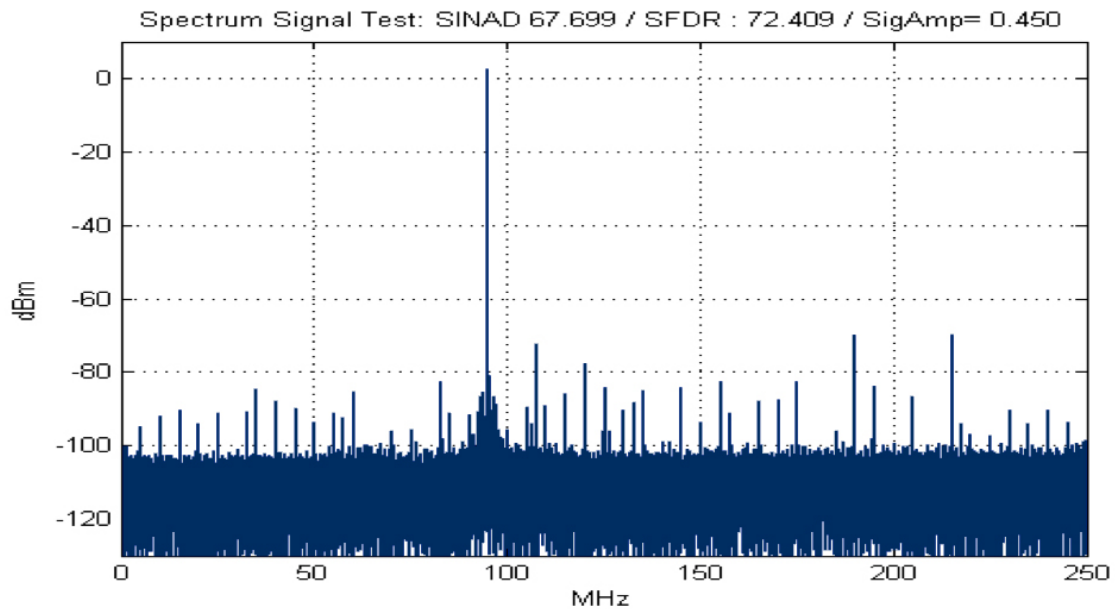


Figure 7. Result from Spectrum Signal Test. Source: [Keysight.com](http://Keysight.com)

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>Reference clock output</b>					
Frequency		10 to 12.5 <sup>1</sup>		MHz	Generated from the internal clock, user selectable
Voltage		800		mV <sub>pp</sub>	On a 50 $\Omega$ load

M3302A-C22					
Power		2		dBm	On a 50 $\Omega$ load
Source impedance		50		$\Omega$	AC coupled
External I/O trigger/marker					
V <sub>IH</sub>	2		5	V	
V <sub>IL</sub>	0		0.8	V	
V <sub>OH</sub>	2.4		3.3	V	On a high Z load
V <sub>OL</sub>	0		0.25	V	On a high Z load
Input impedance		10		K $\Omega$	
Source impedance		TTL		-	
Speed		100		MHz	

1 (-CLF) option is set to 10 MHz.

## Data Acquisition Blocks (DAQs) Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
General specifications					
DAQs		2			1 per output channel
Aggregated speed			1000	MSa/s	For all onboard DAQs combined
Acquisition burst multiple		5		Samples	Burst length must be a multiple of this value
Acquisition RAM capacity	15		957M	Samples	Maximum depends on onboard RAM
Acquisition RAM capacity efficiency		93.5		%	Efficiency = waveform size/waveform size in RAM
Trigger		Select			Hardware trigger (analog channels, input trigger, backplane triggers), Software trigger
DAQ specifications					
Speed			500	MSa/s	Per DAQ
Resolution		14		Bits	

## Clock System Specifications

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
General specifications					
Clock Frequency (-CLF)		500		MHz	Fixed Clock

# System Specifications

## Environmental specifications (PXI Express)

M3302A-C22					
Parameter	Min	Typ	Max	Units	Comments
<b>System bus</b>					
Slots		2		Slots	PXI Express (CompactPCI Express compatible)
PCI Express type		Gen 1			Chassis dependent
PCI Express link	1		4	Lanes	Automatic lane negotiation, chassis dependent
<b>Power dissipation</b>					
3.3 V PXIe power supply		3		A	~ 10 W
12 V PXIe power supply		3.5		A	~ 40 W

Environmental <sup>1</sup>		
Temperature range	Operating	0 to +55°C (10,000 feet)
	Non-operating	-40 to +70 °C (up to 15,000 feet)
Max operative altitude		3000 m (10,000 feet)
Operating Humidity range (%RH)		10 to 95% at 40 °C
Non-operating Humidity range (%RH)		5 to 95%
EMC		Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

## Ordering Information <sup>1</sup>

Product	Description
M3302A	PXI Combo: Arbitrary waveform generator: 500 MSa/s, 16 Bits + Digitizer: 500 MSa/s, 14 Bits
Options	Description
M3302A-C22	Two channels AWG + Two channels DIG <sup>2</sup>
M3302A-CLF	Fixed sampling clock, low jitter
M3302A-DM1	Dual modulation capability for the AWG (amplitude and angle simultaneously)
M3302A-M20	Memory 2 GB, 1 GSamples <sup>2</sup>
HW programming options	Description
M3302A-HVI	Enables HVI programming, requires the -HV1 option and the HVI software license (KS2201A)
M3302A-FP1	Enables FPGA programming, requires -K41 option and an FPGA design environment license (KF9000A)
M3302A-K41	FPGA, Xilinx 7K410T, required for -FP1 option only (needs memory option -M20)
Related software <sup>3</sup>	Description
M3601A	HVI design environment
M3602A	FPGA design environment
KS2201A	PathWave Test Sync Executive
KF9000A	PathWave FPGA

1. All options must be selected at time of purchase and are not upgradable.
2. These options represent the standard configuration.
3. M3601A / M3602A are supported with SD1 2.x software only, whereas KS2201A / KF9000A are supported with SD1 3.x software only.

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