DATA SHEET

M3300A PXIe Arbitrary Waveform Generator and Digitizer with Optional Real-Time Sequencing and FPGA Programming

500 MSa/s, 16 Bits, 2/4 Channel Arbitrary Waveform Generator

100 MSa/s, 14 Bits, 4/8 Channel Digitizer

Applications

General purpose AWGs and digitizers

High-performance control

Communications: BB/IF SDR, channel emulation, transceiver testing

Aerospace and defense (A/D): RADAR, electronic warfare (EW)

Hardware-in-the-loop (HIL), automated test equipment (ATE)

Scientific research

Quantum computing

Fast, Flexible, High-Performance Control, Testing & Prototyping

The M3300A modules provide the ideal tool for testing and prototyping in control or communications applications. Performance meets simplicity, thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI), and graphical FPGA programming technology.

KEYSIGHT TECHNOLOGIES

Features

Outputs (AWG)

- 500 MSa/s, 16 Bits, 2/4 Channels

Output features

- AWGs, function generators, AM/FM/PM modulators
- Advanced triggering and marking functionalities

Inputs (Digitizer)

- 100 MSa/s, 14 Bits, 4/8 Channels

Input features

- Powerful data acquisition system (DAQ)
- Advanced triggering and marking functionalities

Less than 400 ns input to output latency

Optional HW programming for high-performance applications

- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7K410T FPGA

Up to 2 GB of onboard RAM (~ 1 Gsamples)

Mechanical/interface

- 2 slots 3U (PXIe)
- PCIe Gen1
- Independent DMA channels for fast and efficient data transfer

Functional Block Diagrams

Output — Arbitrary Waveform Generator

Note that all channels have identical output structure.

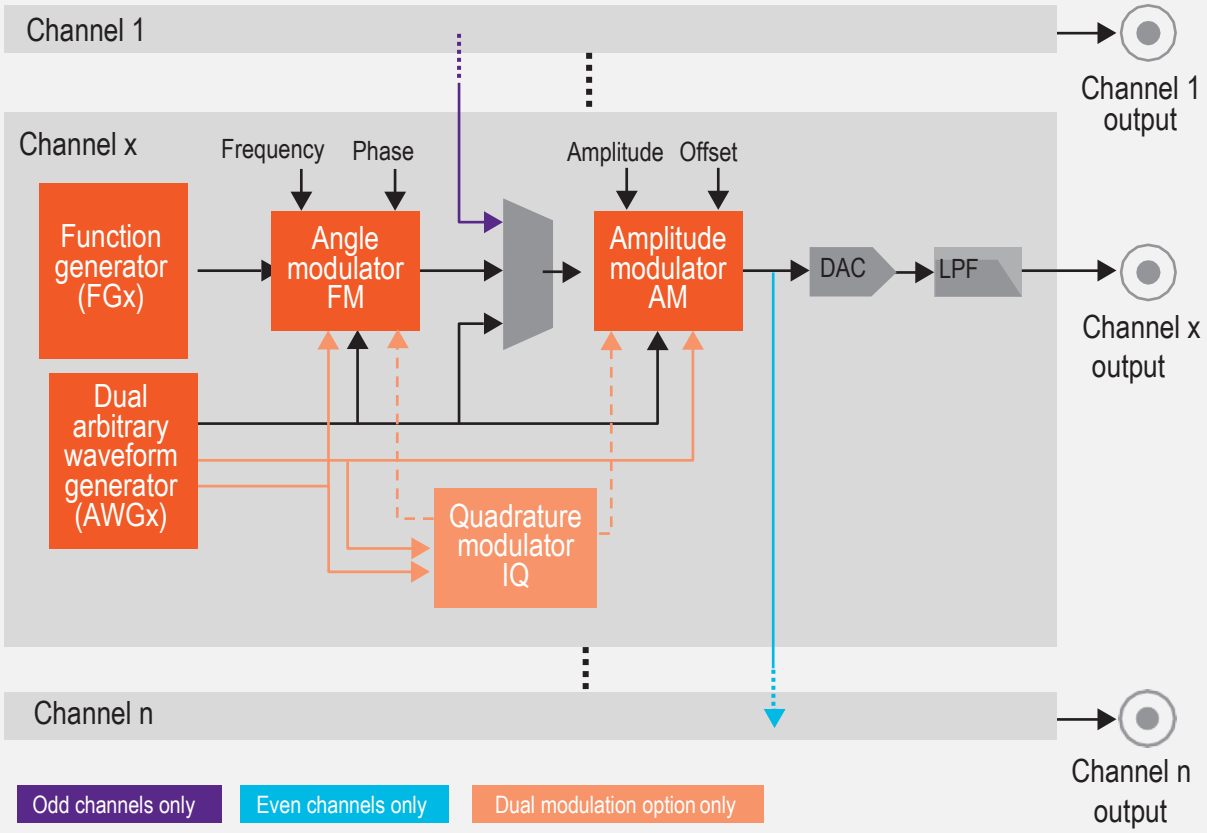

Figure 1. M3300A output functional block diagram. Source: Keysight.com

Input — Digitizer

Note that all channels have identical input structure.

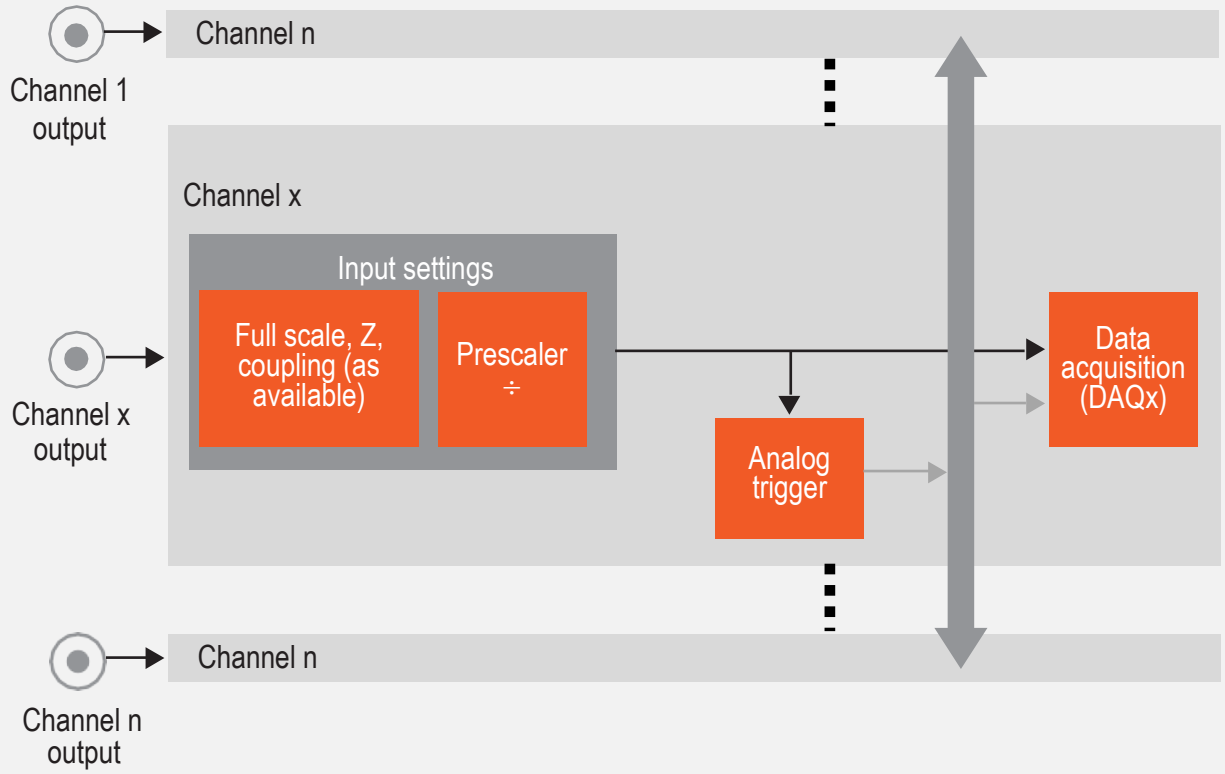

Figure 2. M3300A input functional block diagram. Source: Keysight.com

Programming Technology and Software Tools

Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python

Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully parallel, hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization and data exchange
- FPGA programming
  - FPGA design environment and BSP support
  - Supports VHDL, Verilog and Xilinx projects, and Xilinx IP Catalog
  - Ultra-fast, one-click compiling and on-the-fly programming

SD1 2.x and SD1 3.x differences

Keysight SD1 2.x software has been upgraded to 3.x. The key differences are listed in the table below. For more detail on SD1 3.x software, refer to the Start Up Guide M3xxx-90002.

WARNING **The 3.X version of software does not support programs using the M3601A or the M3602A applications. You will have to transition to KS2201A and KF9000A respectively.**

SD1 Features	Legacy (SD1 2.1.x)	New (SD1 3.x)
Software		
Design Environment	M3601A HVI design environment (ProcessFlow)	KS2201A PathWave Test Sync Executive (HVI2 technology)
	M3602A FPGA design environment (FPGAFlow)	KF9000A PathWave FPGA Programming Environment (commonly known as PathWave FPGA)
HVI Technology[1]	• Graphical M3601A for HV1 • HVI-C API (through SD1 installer)	KS2201A PathWave Test Sync Executive (HVI2 Core API through a separate HVI installer)
FPGA Programming	• Graphical M3602A FPGA Designing (BSP for SD1 2.1.x only)	KF9000A PathWave FPGA (BSP installer for each supported module is required)
Soft Front Panel (SFP)	Available	Available
Programming Interface	Python [1], C++, C#, LabVIEW, MATLAB	Python [1], C, C++, C#, LabVIEW, MATLAB
Supported Operating System	Windows 10 (32 / 64 bit)	Windows 10 (x64 bit)
Hardware modules		
M3202A (AWG 1G)	FW version<4.0 (CH2* or CH4) (CLF / CLV) (K16, K32, K41) BSP available (K32,K41)	FW version>=4.0 (CH4) (CLF / CLV**) (K16, K32, K41) BSP available(K32, K41)
M3201A (AWG 500)	FW version<4.0 (CH2* or CH4) (CLF / CLV) (K16, K32, K41) BSP available (K32, K41)	FW version>=4.0 (CH4) (CLF / CLV**) (K16, K32, K41) BSP available (K32, K41)

SD1 Features	Legacy (SD1 2.1.x)	New (SD1 3.x)
M3102A (DIG 500)	FW version<2.0 (CH2* or CH4) (CLF / CLV*) (K16, K32, K41) BSP available (K32, K41)	FW version>=2.0 (CH4) (CLF) (K16, K32, K41) BSP available(K32, K41)
M3100A (DIG 100)	FW version<2.0 (CLF / CLV*) (CH4 or CH8) (K16, K32, K41) BSP available (K32, K41)	FW version>=2.0 (CLF) (CH4 or CH8) (K32, K41) BSP available (K32, K41)
M3302A (COMBO 500 500)	FW version<4.0 (CLF / CLV*) (CH2 AWG–CH2 DIG) (K32*, K41) BSP available (K32*, K41)	FW version>=4.0 (CLF) (CH2 AWG–CH2 DIG) (K41) BSP available (K41)
M3300A (COMBO 500 100)	FW version<4.0 (CLF) (CH2 AWG–CH4 DIG or CH4 AWG–CH8 DIG) (K16*, K32*, K41) BSP available (K32*)	FW version>=4.0 (CLF) (CH2 AWG–CH4 DIG or CH4 AWG–CH8 DIG) (K41) BSP available (K41)
No programming		
Easily configurable SD1 SFP (software front panel) interface for each connected module.		

1 HVI programming with supported with Python version 3.7 only.

* This Hardware Option cannot be procured. Contact Keysight Support for more information.

** Only Default Clock Speed is supported. Variable Clock is NOT supported.

PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

Product	Type	Output (AWGs)				Input (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	4	DC-400				
M3201A	AWG	500	16	4	DC-200				
M3102A	Digitizer					500	14	4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	DC-200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	DC-200	100	14	4/8	DC-100

AWG Technical Specifications and Characteristics

General characteristics

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Inputs and Outputs								
Channels (single-ended mode)		2			4		Out	
Channels (differential mode)		1			2		Out	Differential uses 2 channels
Reference clock [1]		1			1		Out	
Reference clock [2]		1			1		In	
Triggers/markers [1, 3]		1			1		In/Out	Reconfigurable
Triggers/markers [2, 3]		8			8		In/Out	Reconfigurable
Output channels overview								
Sampling rate		500			500		Msa/s	Fixed sampling clock
Voltage resolution		16			16		Bits	
Output frequency	DC		200	DC		200	MHz	
Real-time BW			200			200	MHz	
Output voltage	-1.5		1.5	-1.5		1.5	Volts	
Built-in functionalities								
Function generators		2			4			1 per channel
Dual AWGs		2			4			1 per channel
IQ modulators		2			4			1 per channel
Frequency modulators		2			4			1 per channel
Phase modulators		2			4			1 per channel
Amplitude modulators		2			4			1 per channel
DC offset modulators		2			4			1 per channel
Onboard memory								
RAM memory	16		2048	16		2048	MBytes	

1. At front panel.
2. At backplane.
3. Markers available from SD1 software version 3.0 onwards.

I/O Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Output channels								
Sampling rate		500			500		MSa/s	Fixed sampling clock
Output frequency	DC		200	DC		200	MHz	Limited by a reconstruction filter
Output voltage	-1.5		1.5	-1.5		1.5	Volts	On a 50 Ω load
Source impedance		50			50		Ω	
Reference clock output								
Frequency		10 or 100			10 or 100		MHz	Generated from the internal clock, user selectable
Voltage		800			800		mV_{pp}	On a 50 Ω load
Power		2			2		dBm	On a 50 Ω load
Source impedance		50			50		Ω	AC coupled
External I/O trigger/marker								
V_{IH}	2		5	2		5	V	
V_{IL}	0		0.8	0		0.8	V	
V_{OH}	2.4		3.3	2.4		3.3	V	On a high Z load
V_{OL}	0		0.5	0		0.5	V	On a high Z load
Input impedance		10			10		KΩ	
Source impedance		TTL			TTL		-	
Speed			500			500	MHz	

Function Generators (FGs) Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
Function generators		2			4			1 per channel
Waveform types		4			4			Sinusoidal, triangular, square and DC
Frequency range	0		200	0		200	MHz	
Frequency resolution		45			45		Bits	
Frequency resolution		5.7			5.7		µHz	
Phase range	0		360	0		360	Deg	
Phase resolution		24			24		Bits	
Phase resolution		21.5			21.5		µdeg	
Reference clock output								
Frequency change rate			100			100	MChanges/s	With HVI technology
Frequency modulation rate			500			500	MSamples/s	With AWGs and angle modulators
Phase change rate			100			100	MChanges/s	With HVI technology
Phase modulation rate			500			500	MSamples/s	With AWGs and angle modulators

Amplitude and Offset Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
Amplitude/offset range	-1.5		1.5	-1.5		1.5	Volts	Amplitude + offset values
Amplitude/offset resolution		16			16		Bits	
Amplitude/offset resolution		45.8			45.8		µV	
Reference clock output								
Amplitude/offset change rate			500			500	MChanges/s	With HVI technology
Amplitude/offset modulation rate			500			500	MSamples/s	With AWGs and angle modulators

Arbitrary Waveform Generators (AWGs) Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
Dual AWGs		2			4			1 Dual AWG per output channel
Aggregated speed (16 bits)			2000			4000	MSa/s	For all onboard waveforms combined
Aggregated speed (32 bits)			1000			2000	MSa/s	For all onboard waveforms combined
Waveform multiple		5			5		Samples	Waveform length must be a multiple of this value
16-bit waveform length	65		957M	15		957M	Samples	Maximum depends on onboard RAM
32-bit waveform length	65		478M	10		478M	Samples	Maximum depends on onboard RAM
Waveform length efficiency		93.5			93.5		%	Efficiency = waveform size/waveform size in RAM
Trigger		Select			Select			External Trigger (input connector, backplane triggers), SW/HVI trigger
AWG specifications (16-bit single waveform)								
Speed			500			500	MSa/s	Per AWG
Resolution		16			16		Bits	
AWG destination		Select			Select			Amplitude, offset, frequency or phase
AWG specifications (16-bit dual waveform)								
Speed (waveform A)			500			500	MSa/s	Per AWG
Speed (waveform B)			500			500	MSa/s	Per AWG
Resolution (waveform A)		16			16		Bits	
Resolution (waveform B)		16			16		Bits	
AWG destination (waveform A)		Select			Select			Amplitude and offset or I and Q control outputs on channels 1,2
AWG destination (waveform B)		Select			Select			Frequency and phase or I and Q readouts on channels 3,4

Angle Modulators Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
Frequency modulators		2			4			1 per output channel
Phase modulators		2			4			1 per output channel
Carrier signal source		FGs			FGs			refer FG specifications table in this document
Modulating signal source		AWGs			AWGs			refer AWG specifications table in this document
Frequency modulators (16-bit modulating waveform)								
Deviation	-Dev. Gain		+Dev. Gain	-Dev. Gain		+Dev. Gain	MHz	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		200	0		200	MHz	
Deviation gain resolution		16			16		Bits	
Phase modulators (16-bit modulating waveform)								
Deviation	-Dev. Gain		+Dev. Gain	-Dev. Gain		+Dev. Gain	Deg	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		180	0		180	Deg	
Deviation gain resolution		16			16		Bits	~ 5.5 mdeg

Amplitude Modulators Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
Amplitude modulators		2			4			1 per output channel
Offset modulators		2			4			1 per output channel
Carrier signal source		FGs			FGs			refer FG specifications table in this document
Modulating signal source		AWGs			AWGs			refer AWG specifications table in this document
Amplitude and offset modulators (16-bit modulating waveform)								
Deviation	-Dev. Gain		+Dev. Gain	-Dev. Gain		+Dev. Gain	V_p	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		1.5	0		1.5	V_n	
Deviation gain resolution		16			16		Bits	Limited by the output DAC

IQ Modulators Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
IQ modulators		2			2			1 per output channel
Carrier signal source		FGs			FGs			refer FG specifications table in this document
Modulating signal source		AWGs			AWGs			refer AWG specifications table in this document
External I/O trigger/marker								
Amplitude deviation	-1.5		+1.5	-1.5		+1.5	V_p	
Phase deviation	-180		180	-180		180	Deg	
I modulating signal resolution		16			16		Bits	AWG waveform
I modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Q modulating signal resolution		16			16		Bits	AWG waveform
Q modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit

Clock System Specifications

	M3300A-C24			M3300A-C48				
Parameter	Min	Typ	Max	Min	Typ	Max	Units	Comments
General specifications								
Clock Frequency (-CLF)		500			500		MHz	Fixed Clock

AC performance

	M3300A-C24			M3300A-C48				
Parameter	Min	Typ	Max	Min	Typ	Max	Units	Comments
General characteristics								
Analog output jitter			< 2			< 2	ps	RMS (cycle-to-cycle)
AWG trigger to output jitter			< 2			< 2	ps	RMS (cycle-to-cycle) for any trigger referenced to the chassis clock; independent of input trigger jitter if input, jitter < 4ns peak-to-peak
Trigger resolution		10			10		ns	
Channel-to-channel skew			< 20			< 20	ps	Between ch 0 and ch 1, and ch 2 and ch 3
			< 50			< 50	ps	Between any channel
			150			150	ps	Between modules, chassis dependent [2]
Clock output jitter			< 2			< 2	ps	RMS (cycle-to-cycle)
Clock accuracy and stability			25			25	ppm	PXIe, PCIe versions; chassis dependent [1]
AC characteristics								
Spurious-free dynamic range (SFDR)								
								P_{out} = 4 dBm, measured from DC to max frequency
f_{out} = 10 MHz		68			68		dBc	
f_{out} = 80 MHz		64			64		dBc	
f_{out} = 120 MHz		57			57		dBc	
f_{out} = 160 MHz		54			54		dBc	
Crosstalk (adjacent channels)								
f_{out} = 10 MHz		< –105			< –105		dB	
f_{out} = 40 MHz		-85			-85		dB	
f_{out} = 80 MHz		–75			–75		dB	
f_{out} = 120 MHz		–88			–88		dB	

	M3300A-C24			M3300A-C48			
f_{out} = 160 MHz		–73			–73		dB	
f_{out} = 200 MHz		-85			-85		dB	
Crosstalk (non-adjacent channels)								
f_{out} = 10 MHz		< –105			< –105		dB	
f_{out} = 40 MHz		< –105			< –86		dB	
f_{out} = 80 MHz		–78			–78		dB	
f_{out} = 120 MHz		< –105			< –105		dB	
f_{out} = 160 MHz		–92			–92		dB	
f_{out} = 200 MHz		–100			–100		dB	
Phase noise (SSB)								
offset = 1 KHz		< –127			< –127		dBc/Hz	
offset = 10 KHz		< –133			< –133		dBc/Hz	
offset = 100 KHz		< –138			< –138		dBc/Hz	
Average noise power density								
		< –142			< –142		dBm/Hz	

1. This value corresponds to a M9505A chassis. This value can be improved with an external chassis clock or a system timing module.
2. This value corresponds to a M9005A PXIe chassis.

AC performance, typical

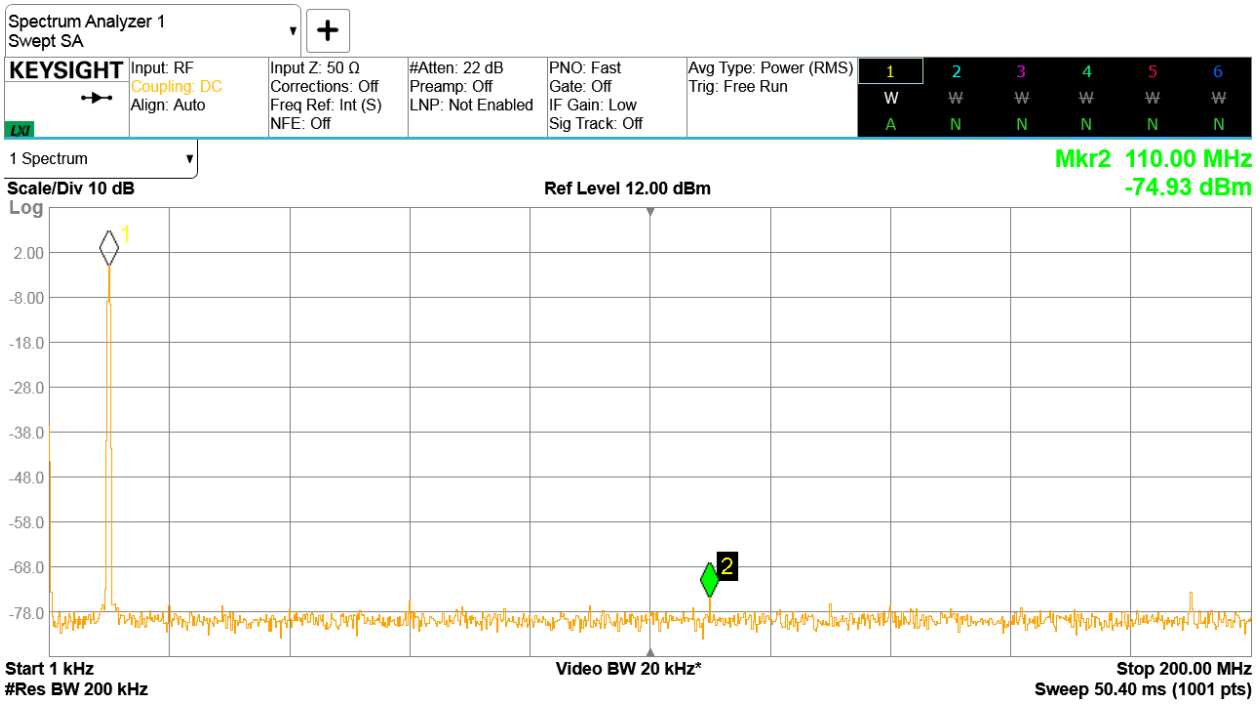

Figure 3. Single-tone spectrum at f_{out} = 10 MHz. Source: Keysight.com

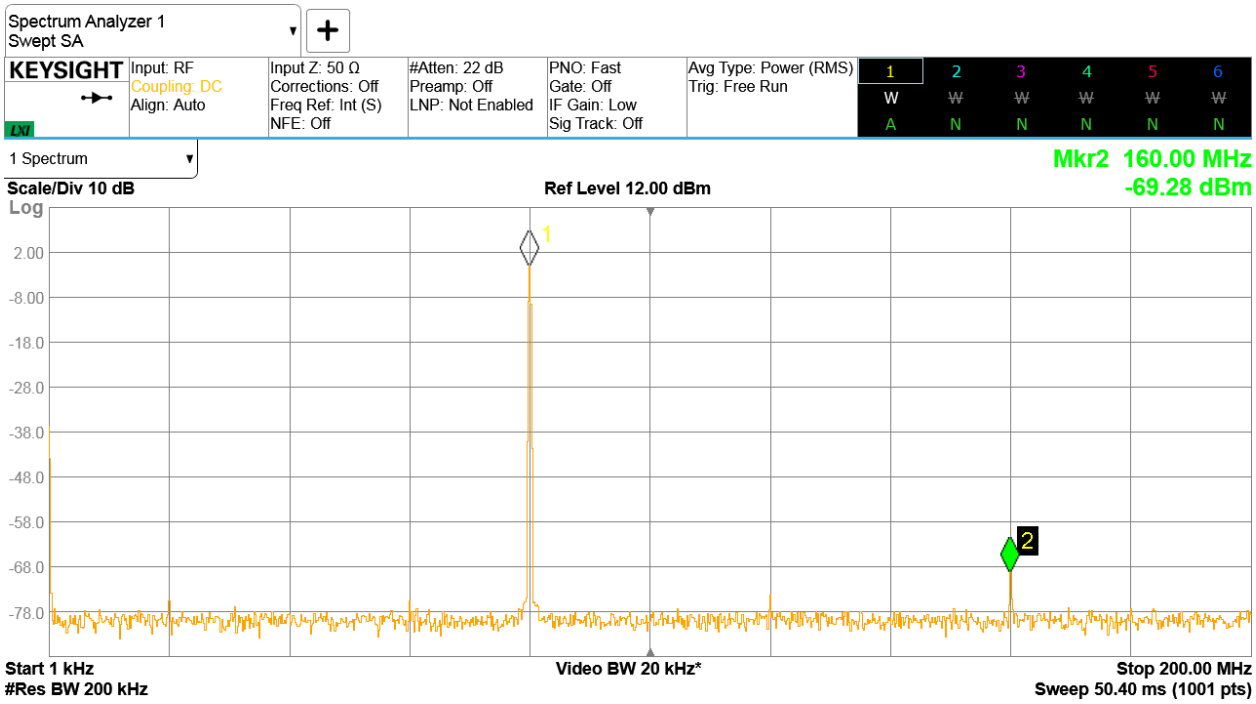

Figure 4. Single-tone spectrum at f_{out} = 80 MHz. Source: Keysight.com

AC performance, typical

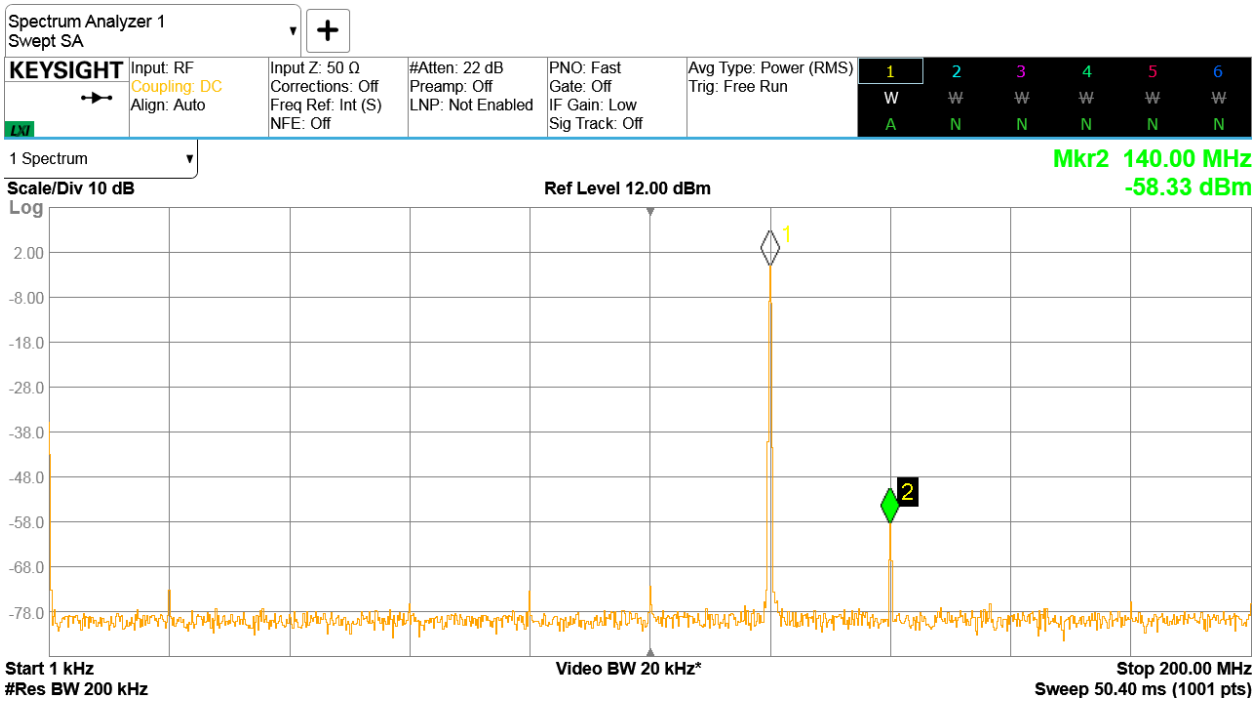

Figure 5. Single-tone spectrum at f_{out} = 120 MHz. Source: Keysight.com

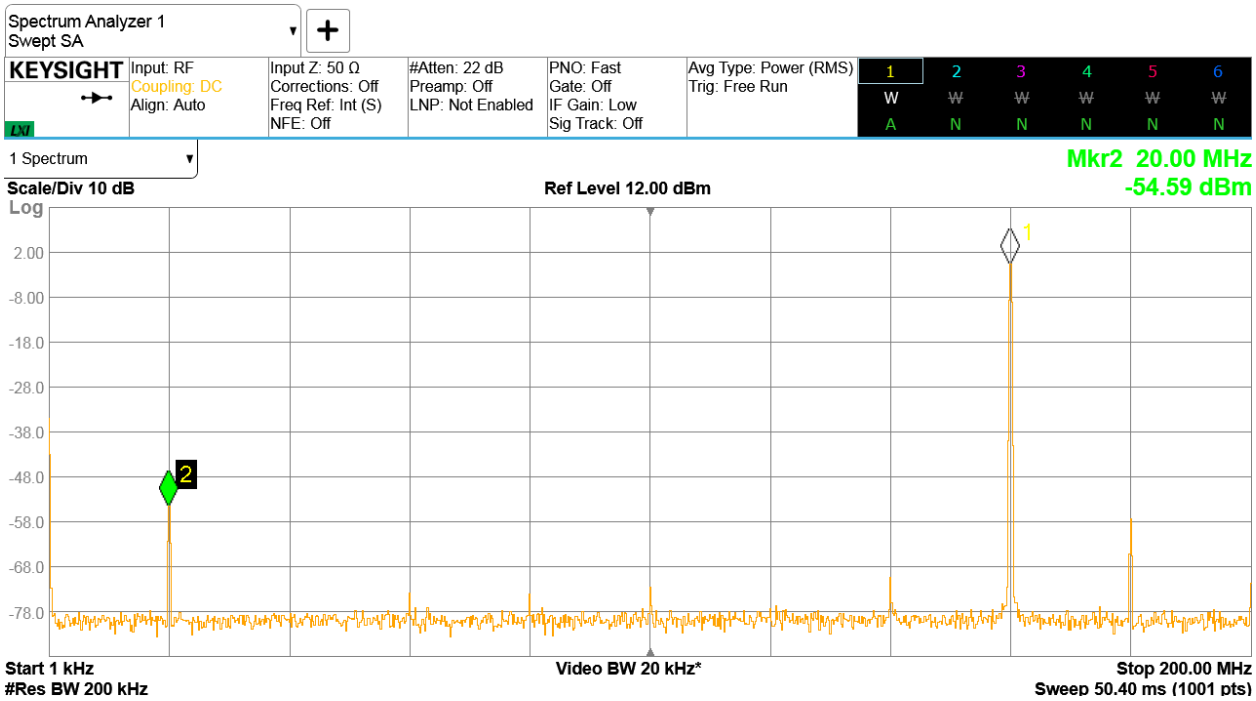

Figure 6. Single-tone spectrum at f_{out} = 160 MHz. Source: Keysight.com

Digitizer Technical Specifications and Characteristics

General characteristics

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Inputs and Outputs								
Channels		4			8		Out	
Reference clock [1]		1			1		Out	
Reference clock [2]		1			1		In	
Triggers/markers [1, 3]		1			1		In/Out	Reconfigurable
Triggers/markers [2, 3]		8			8		In/Out	Reconfigurable
Output channels overview								
Sampling rate		100			100		Msa/s	
Voltage resolution		14			14		Bits	
Input frequency [4]	DC		100	DC		100	MHz	
Real-time BW		50			50		MHz	
Built-in functionalities								
Input conditioning blocks		4			8			1 per channel
Analog trigger processors		4			8			1 per channel
Data acquisition blocks		4			8			1 per channel
Onboard memory								
RAM memory	16		2048	16		2048	MBytes	

1. At front panel.
2. At backplane.
3. Markers available from SD1 software version 3.0 onwards.
4. 100 MHz refer to the Front-End bandwidth. This digitizer can operate in 1st and 2nd Nyquist zones (using undersampling technique), but its real-time BW is limited by Nyquist to some 50 MHz. As an example for a band-limited signal of 70 MHz with a 10 MHz signal bandwidth, the aliased component will appear between 25 to 35 MHz (30 ± 5 MHz).

I/O Specifications

Analog input characteristics	
Number of channels	C24 or C48
Sampling rate	100 MSa/s option -CLF
Configurable inputs: impedance	50 Ω or 1 MΩ (HiZ)
Configurable inputs: Coupling	AC or DC
Input voltage range (50 Ω)	400 mV_{pp} to 6 V_{pp} (continuous variable attenuator at input)
Input voltage range (HiZ)	200 mV_{pp} to 20 V_{pp} (continuous variable attenuator at input)
Bandwidth limit filters	100 MHz
Effective number of bits (ENOB)	10.8 bits at 30 MHz (typical)
Noise floor	–142 dBm/Hz at 30 MHz (typical)
SINAD	67 dB at 30 MHz (typical)
Spurious free dynamic range (SFDR) + Total Harmonic Distortion	79 dBc (typical)

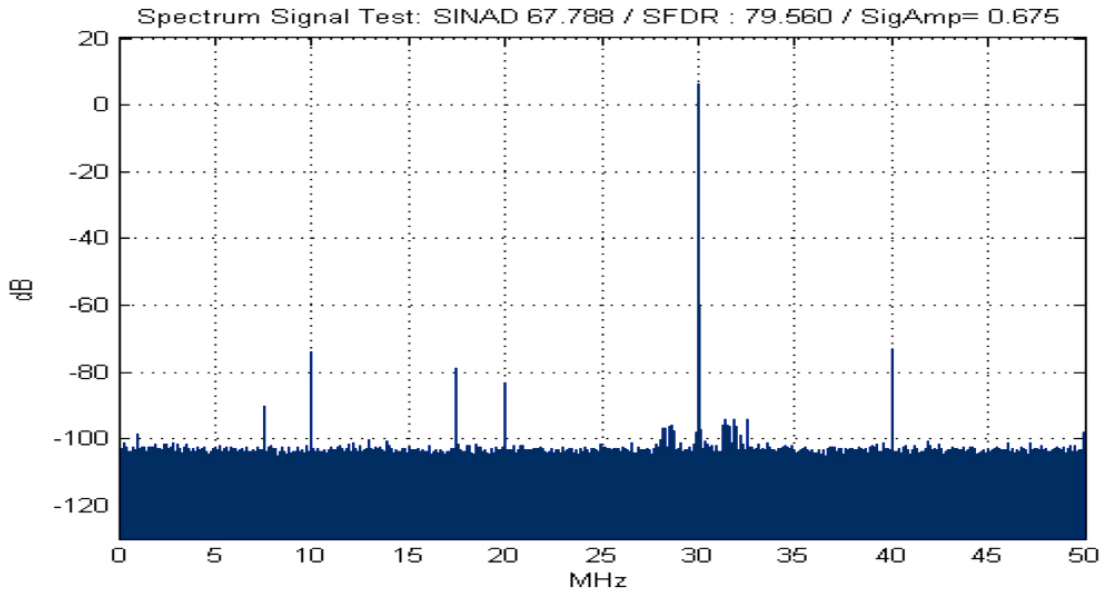

Figure 7. Result from Spectrum Signal Test. Source: Keysight.com

M3300A					
Parameter	**Min**	**Typ**	**Max**	**Units**	**Comments**
Reference clock output					
Frequency		10 or 100		MHz	Generated from the internal clock, user selectable
Voltage		800		mV_{pp}	On a 50 Ω load

M3300A					
Power		2		dBm	On a 50 Ω load
Source impedance		50		Ω	AC coupled
External I/O trigger/marker					
V_{IH}	2		5	V	
V_{IL}	0		0.8	V	
V_{OH}	2.4		3.3	V	On a high Z load
V_{OL}	0		0.5	V	On a high Z load
Input impedance		10		KΩ	
Source impedance		TTL		-	
Speed			500	MHz	

Data Acquisition Blocks (DAQs) Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
DAQs		4			8			1 per output channel
Aggregated speed			400			800	MSa/s	For all onboard DAQs combined
Acquisition burst multiple		5			5		Samples	Burst length must be a multiple of this value
Acquisition RAM capacity	15		957M	15		957M	Samples	Maximum depends on onboard RAM
Acquisition RAM capacity efficiency		93.5			93.5		%	Efficiency = waveform size/waveform size in RAM
Trigger		Select			Select			Hardware trigger (analog channels, input trigger, backplane triggers), Software trigger
DAQ specifications								
Speed			100			100	MSa/s	Per DAQ
Resolution		14			14		Bits	

Clock System Specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
General specifications								
Clock Frequency (-CLF)		100			100		MHz	

System Specifications

Environmental specifications (PXI Express)

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
System bus								
Slots		2			2		Slots	PXI Express (CompactPCI Express compatible)
PCI Express type		Gen 1			Gen 1			Chassis dependent
PCI Express link	1		4	1		4	Lanes	Automatic lane negotiation, chassis dependent
PCI Express speed	400		1600	400		1600	MBytes/s	Depends on # of lanes, chassis, congestion
Power dissipation								
3.3 V PXIe power supply		3			3		A	~ 10 W
12 V PXIe power supply		3.5			3.5		A	~ 40 W

Environmental [1]		
Temperature range	Operating	0 to +55°C (10,000 feet)
	Non-operating	–40 to +70 °C (up to 15,000 feet)
Max operative altitude		3000 m (10,000 feet)
Operating Humidity range (%RH)		10 to 95% at 40 °C
Non-operating Humidity range (%RH)		5 to 95%
EMC		Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device is in compliance with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada This ISM device is in compliance with Australian and New Zealand RCM This ISM device is in compliance with South Korea EMC KCC

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

Ordering Information [1]

Product	Description
M3300A	PXI Combo: Arbitrary waveform generator: 500 MSa/s, 16 Bits + Digitizer: 100 MSa/s, 14 Bits
Options	**Description**
M3300A-C24 / -C48	Two channels AWG + four channels DIG [2] / four channels AWG + eight channels DIG
M3300A-CLF	Fixed sampling clock, low jitter [2]
M3300A-DM1	Dual modulation capability for the AWG (amplitude and angle simultaneously)
M3300A-M20	Memory 2 GB, 1 GSamples [2]
HW programming options	**Description**
M3300A-HVI	Enables HVI programming, requires the -HV1 option and the HVI software license (KS2201A)
M3300A-FP1	Enables FPGA programming, requires -K41 option and an FPGA design environment license (KF9000A)
M3300A-K41	FPGA, Xilinx 7K410T, required for -FP1 option only (needs memory option -M20)
Related software [3]	**Description**
M3601A	HVI design environment
M3602A	FPGA design environment
KS2201A	PathWave Test Sync Executive
KF9000A	PathWave FPGA

1. All options must be selected at time of purchase and are not upgradable.
2. These options represent the standard configuration.
3. M3601A / M3602A are supported with SD1 2.x software only, whereas KS2201A / KF9000A are supported with SD1 3.x software only.

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